Transformer Isolation Signal Conditioning Card

User Manual

CQ9500-TR-08

Concurrent Real-Time 800 Northwest 33rd Street Pompano Beach, FL 33064	Document Number	0810005
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Revision History

Revision	Date	Author	Changes
A.1	03/18/2025	Jim Millener	UM Initial Release
A.2		Jim Millener	Added detail on host interface to Concurrent Real-Time analog boards.

TABLE OF CONTENTS

1. Introduction

This document describes the design and operational aspects of the Concurrent Real-Time CQ9500-TR-08 Configurable Transformer Isolation Signal Conditioning Board.

2. Product Description

2.1 Overview

The CQ9500TR-08 Conditioning Module features 32 galvanically isolated 1:1 ratio center tapped transformer channels and is intended to interface to AC signal applications requiring isolation such as LVDT, RVDT, synchro and resolver position sensors and simulators. For simulation applications, the module is intended to support eight excitation input channels with bypass capability as well as sixteen output channels providing eight dual output feedback channels. Each of the sixteen output channels have jumper selectable AC coupling on one side. The connection to both sides of all 32 of the transformers are jumper selectable to be either the full winding or the winding center tap. An external power supply is not required. The CQ9500TR-08 is DIN mount and includes 6′ cable to connect to an analog I/O front end of Concurrent Real-Time analog I/O devices, as shown in Table 1.

CP-FPGA-2	362K LE FPGA Card with Analog IO
CP-FPGA-3	504K LE FPGA Card with Analog IO
CP-ADS6418	64-Channel Analog Input Card
CP-DA3218-D	32-Channel 18-bit Differential Analog Out Card
CP-DA0818-D	8-Channel 18-bit Differential Analog Out Card
CP-DA3218-S	32-Channel 18-bit Single-ended Analog Out Card
CP-DA0818-S	8-Channel 18-bit Single-ended Analog Out Card
CP-FPGA-4	480K LE FPGA Card with CD-FMC-AIAO Daughter Card
CP-FPGA-5	1150K LE FPGA Card with CD-FMC-AIAO Daughter Card
CP-MFIO	16-ch A/D, 16-ch D/A and 96-ch DIO PCIe Card
CP-AD3224-DS	32-ch, 24-bit Delta-Sigma 5V NIST A/D PCIe Card
CP-AD3224-DS-10	32-ch, 24-bit Delta-Sigma 10V NIST A/D PCIe Card

Table 1

The 68-pin interface connector on the transformer board matches up to the connector on a CCRT FPGA board analog I/O port using a standard SCSI cable. If that connection is made, there is IP in the CCRT FPGA Workbench to simulate up to 4 linear or rotary sensors and/or read up to 4 linear or rotary sensors.

Figure 1 shows a block diagram of the board identifying the I/O connectors. Figure 2 is a block diagram of the board showing the locations of the individual channel circuits.

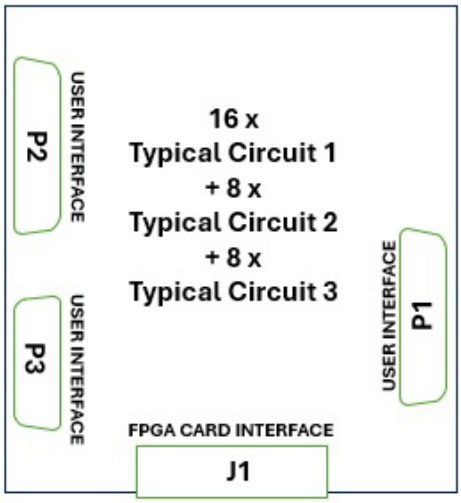


Figure 1

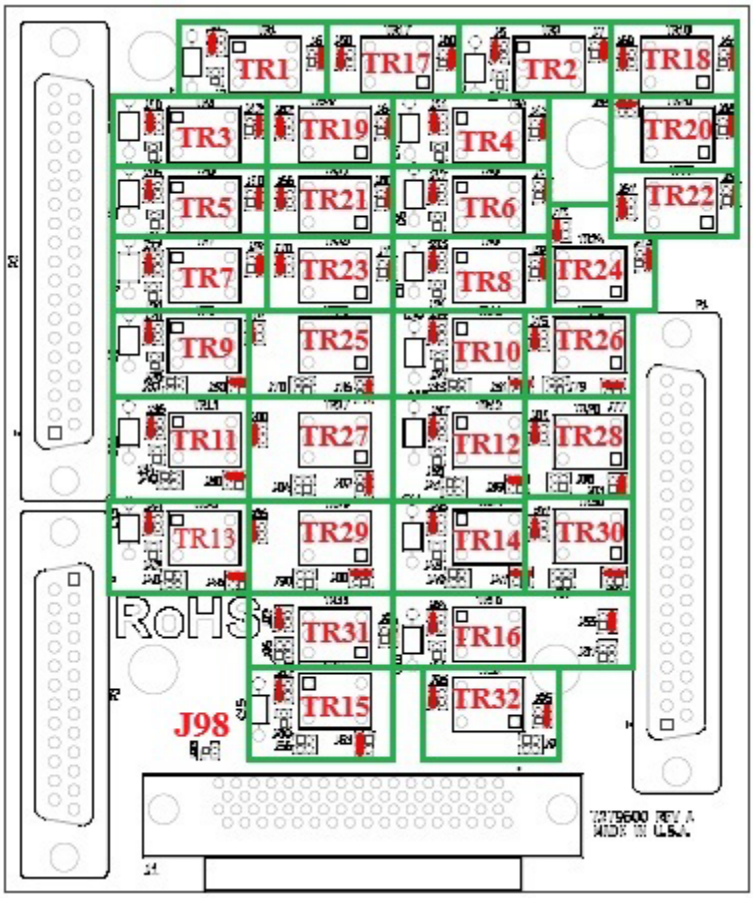
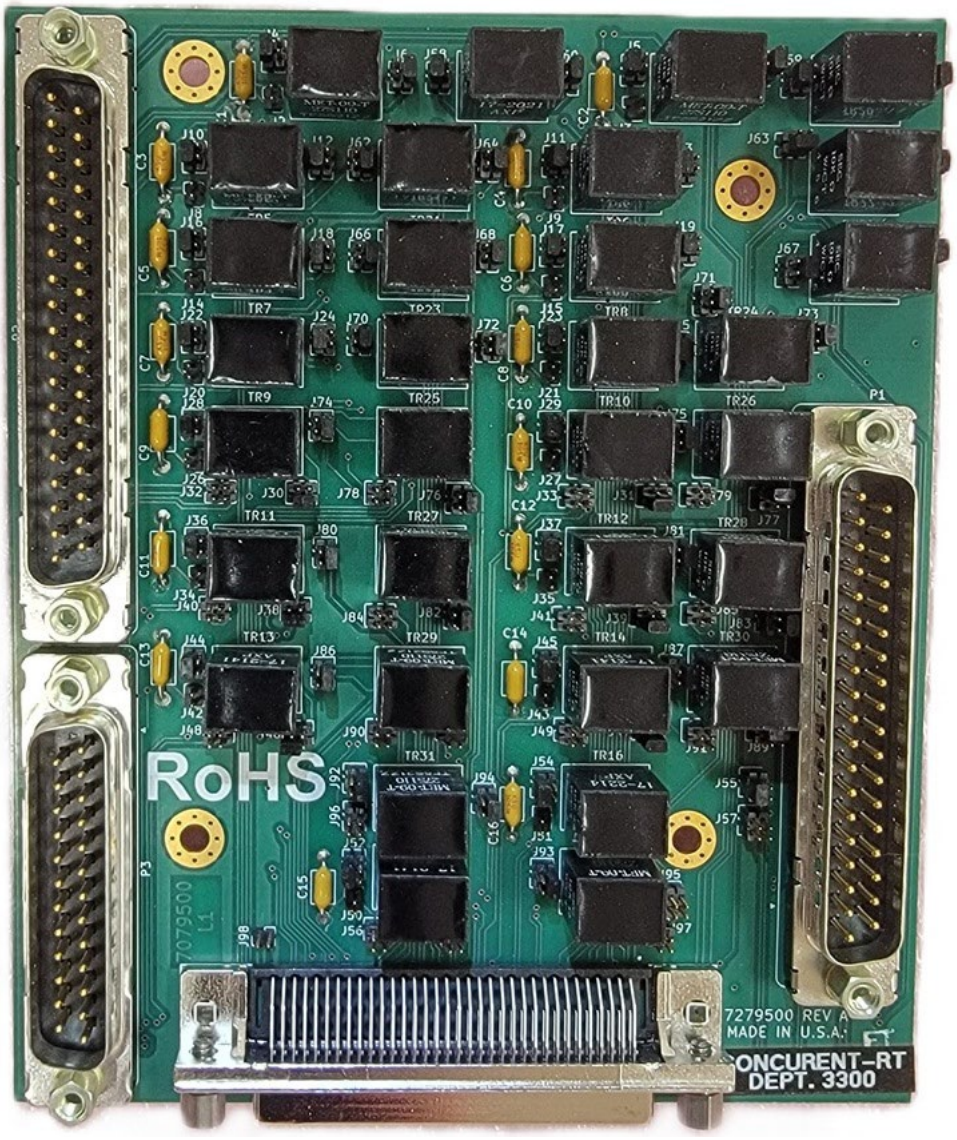


Figure 2

2.2 Picture

Picture 1 is a picture of the DIN mount board assembly.



Picture 1

3. General Operation

The following sections show the general steps required for operation.

3.1 Initial Configuration Setup

1) Before powering on a system with this board in it, configure the jumpers as described in this document to make sure that the I/O is configured as necessary.
2) Connect the SCSI II cable from the FPGA board.
3) Connect user I/O to the D-sub connectors.

3.2 Typical circuit designs

The following four sections describe the typical input and output circuits. Typical schematics as well as board layouts are provided for component locations and jumper references.

3.3 Typical input circuit 0 through 7

The typical input circuit for inputs 0 through 7 is shown in Figure 3

There is a jumper on each circuit to bypass capacitive coupling, J2 in for TR1. Then there is a jumper to connect that side of the transformer to the normal lead or the center tap of the transformer winding, J4 for TR1. There is a jumper that allows the user to select the output from the full secondary winding or the center tap, J6 for TR1. The channels with transformers TR1 – TR8 provide this circuit. The PCB layout for each circuit is provided with reference designator and pin information to assist in locating programming jumper positions. You can zoom in to pictures to see pin jumper numbers.

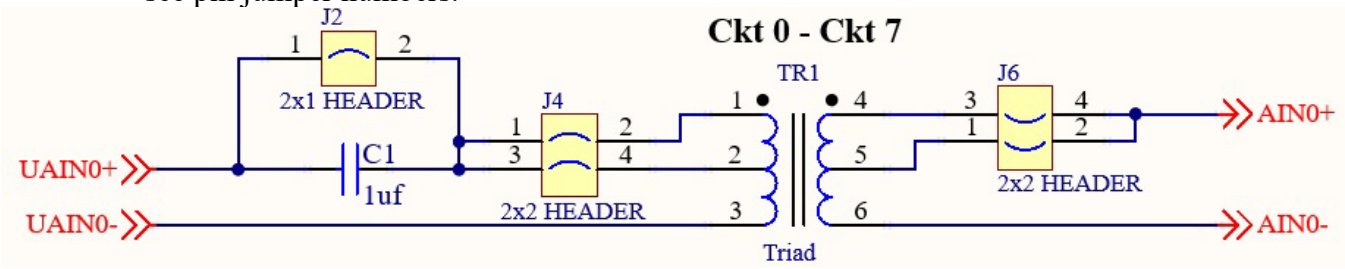
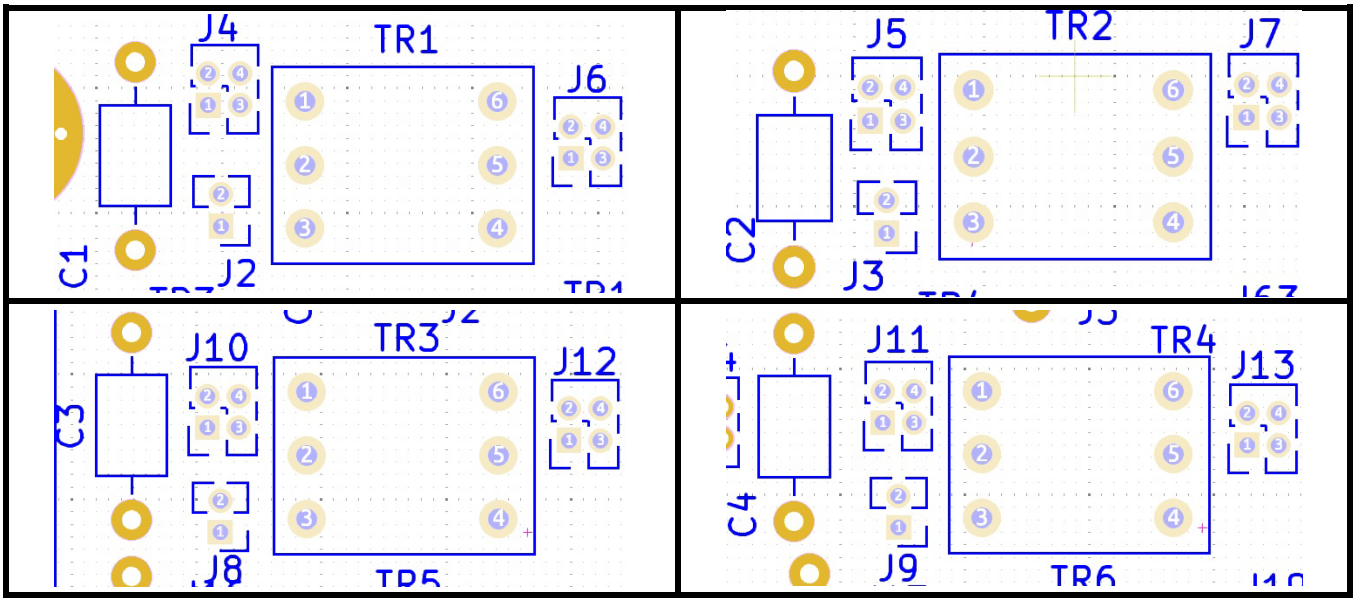
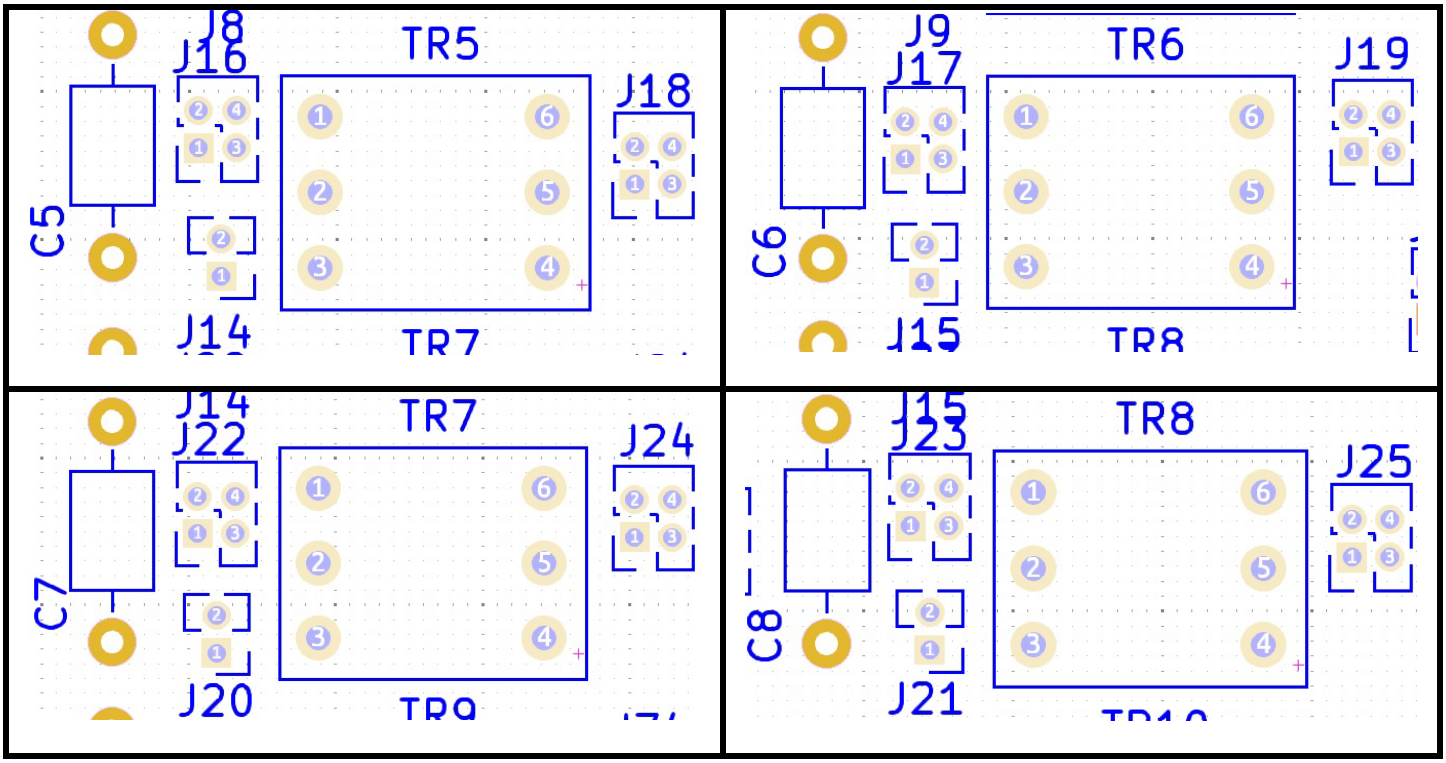


Figure 3





3.4 Typical input circuit 8 through 15

The other typical input circuit for inputs 8 through 15 is shown in Figure 4. This circuit is the same as the other input circuit with the addition of a jumper to bypass the entire circuit, J32 in this case. The channels with transformers TR9 – TR16 provide this circuit. The PCB layout for each circuit is provided with reference designator and pin information to assist in locating programming jumper positions.

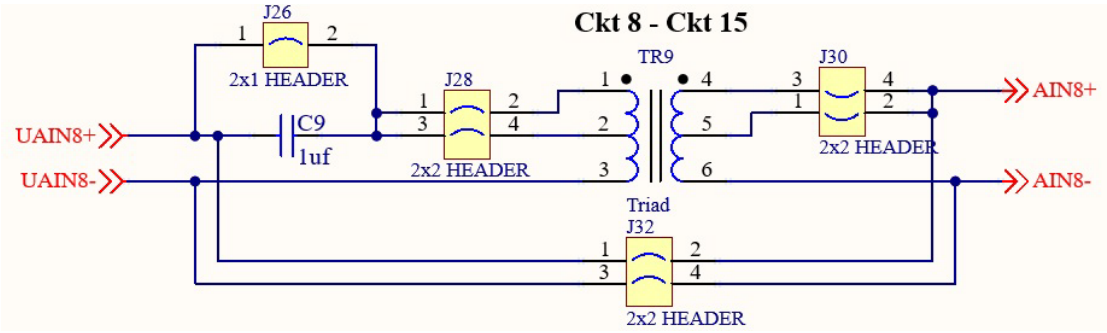
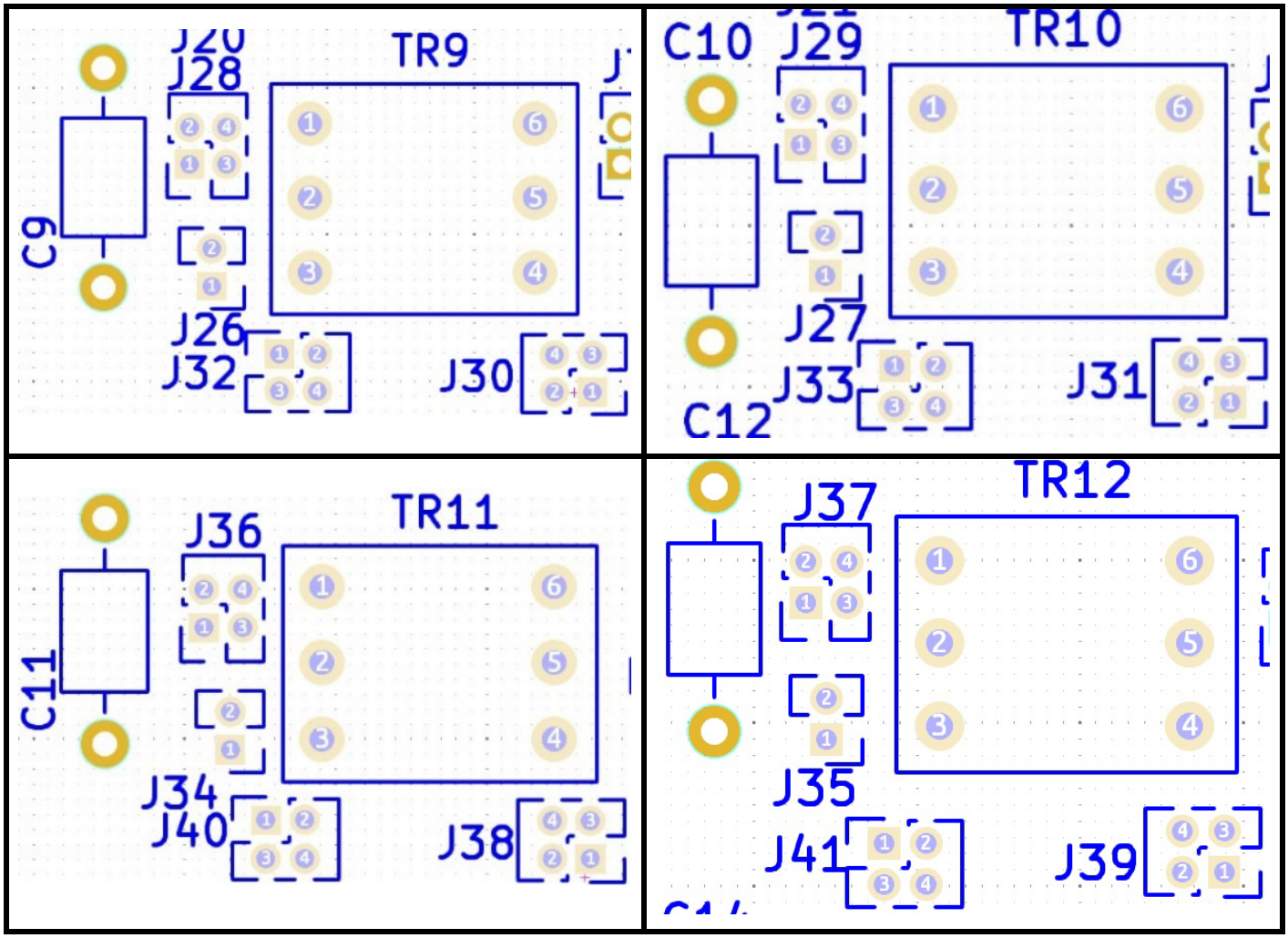
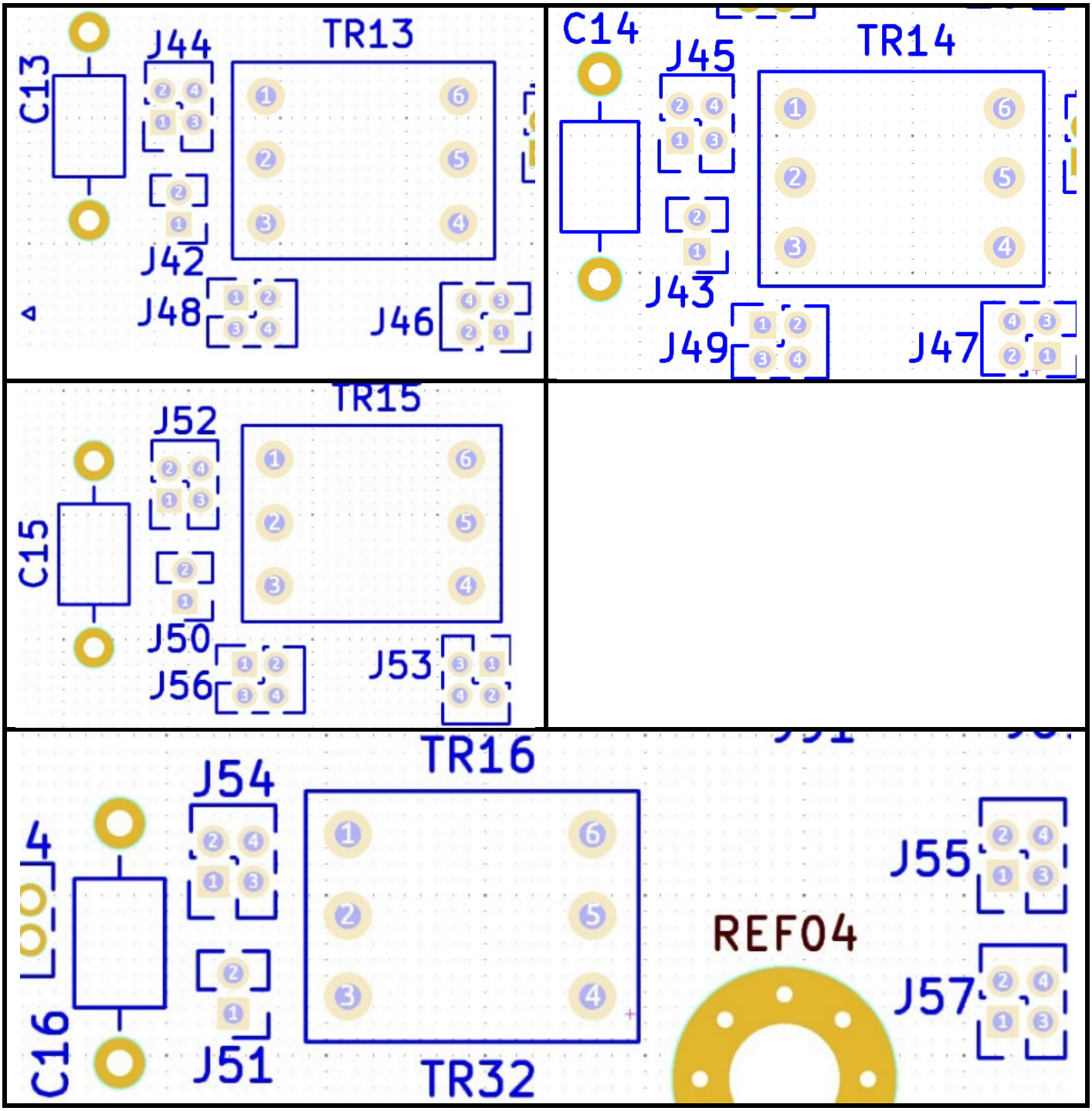


Figure 4





3.5 Typical output circuit 16 through 23

Figure 5 shows the typical output schematic for circuits 16 through 23. There is a jumper to connect each side of the transformer to the normal lead or the center tap of the transformer winding for each circuit. The channels with transformers TR17 – TR24 provide this circuit. The PCB layout for each circuit is provided with reference designator and pin information to assist in locating programming jumper positions.

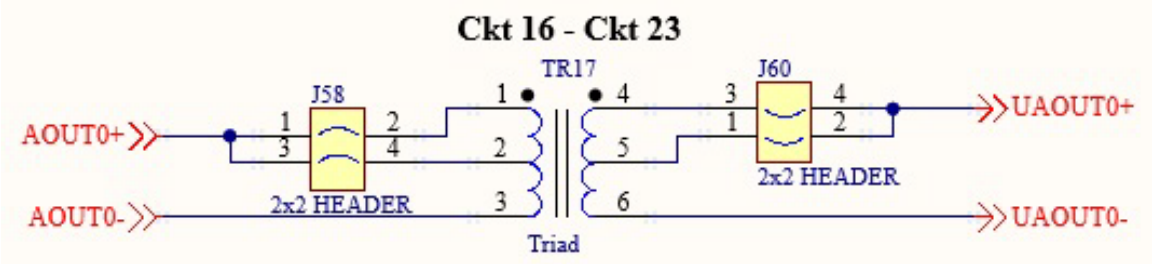
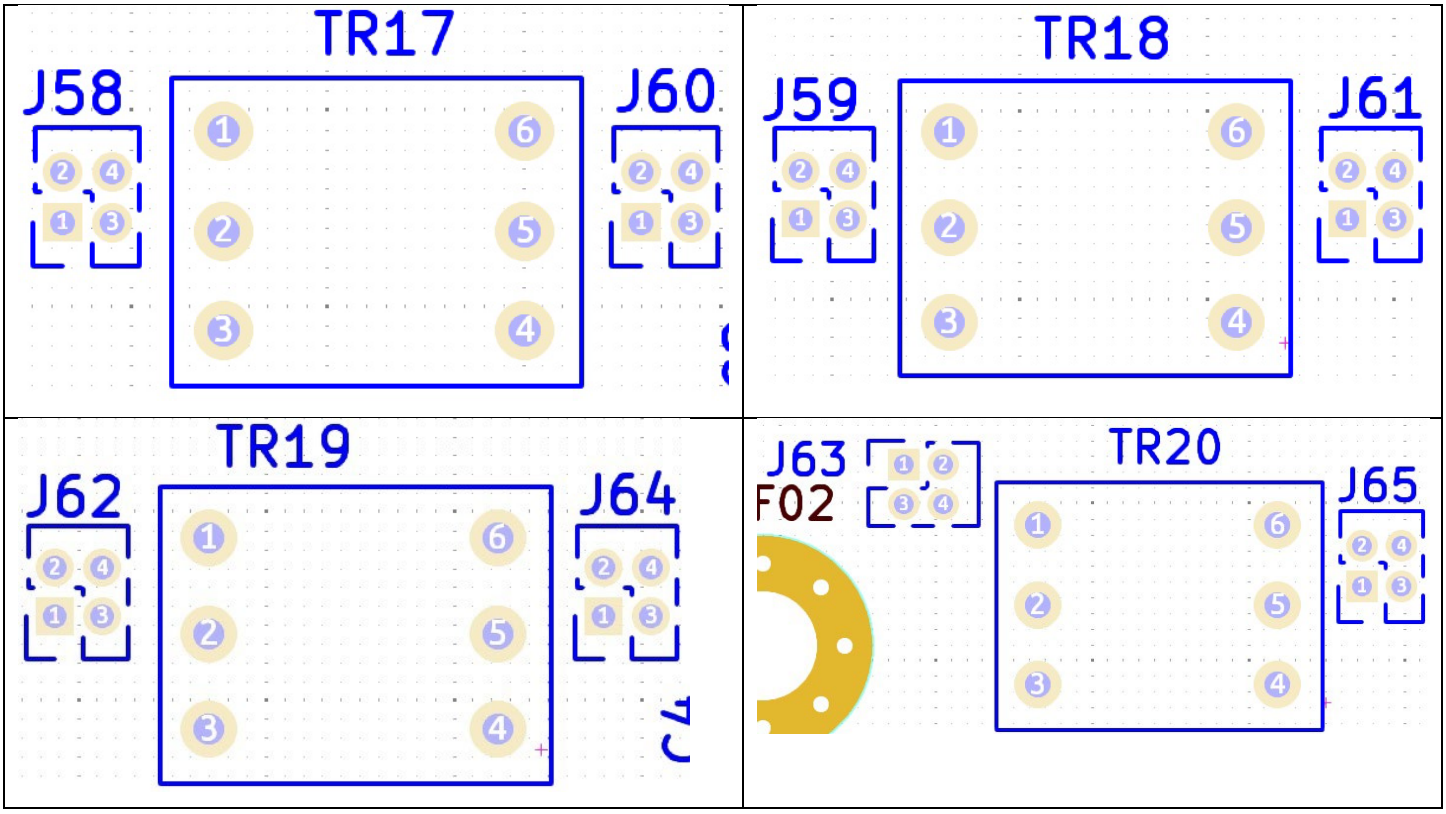
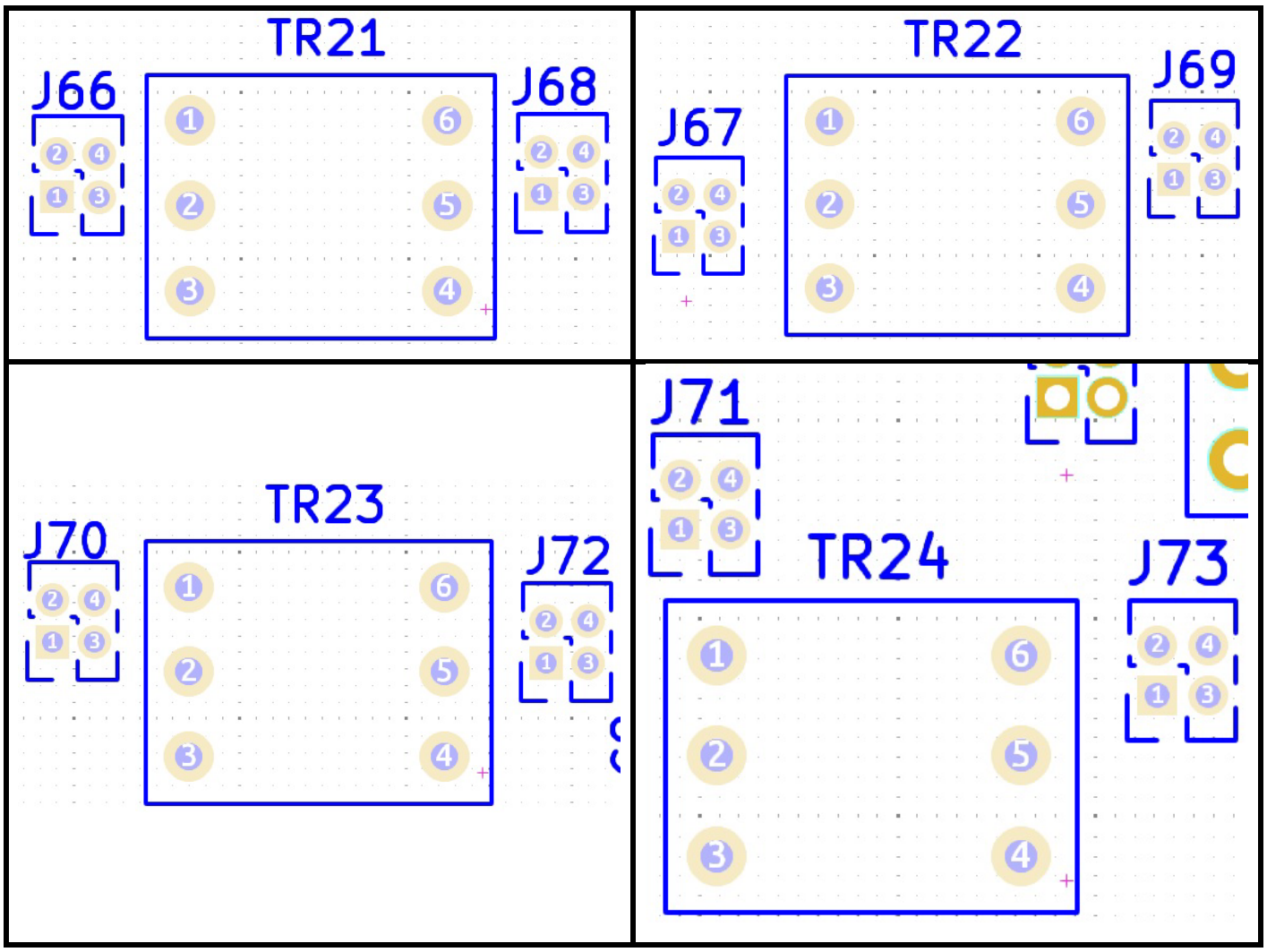


Figure 5





3.6 Typical output circuit 24 through 31

Figure 6 shows the typical output schematic for circuits 24 through 31. This circuit is the same as the other output circuit with the addition of a jumper to bypass the entire circuit, J78 in this case. The channels with transformers TR25 – TR32 provide this circuit. The PCB layout for each circuit is provided with reference designator and pin information to assist in locating programming jumper positions.

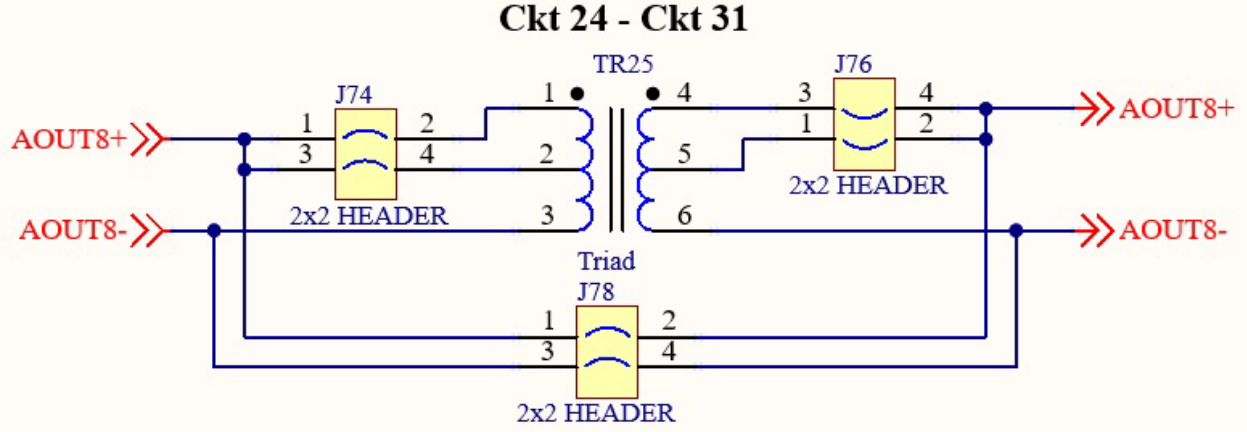
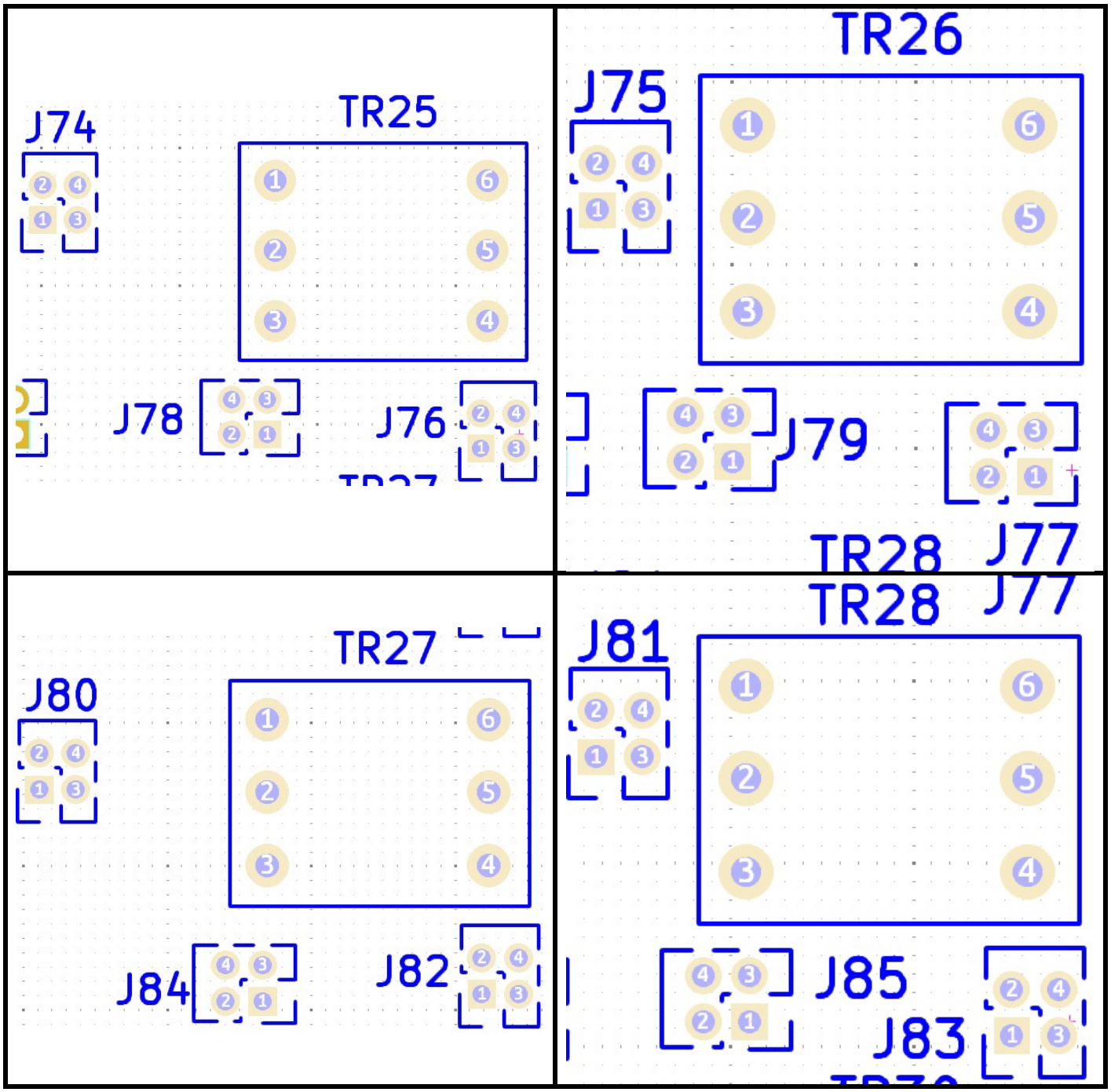
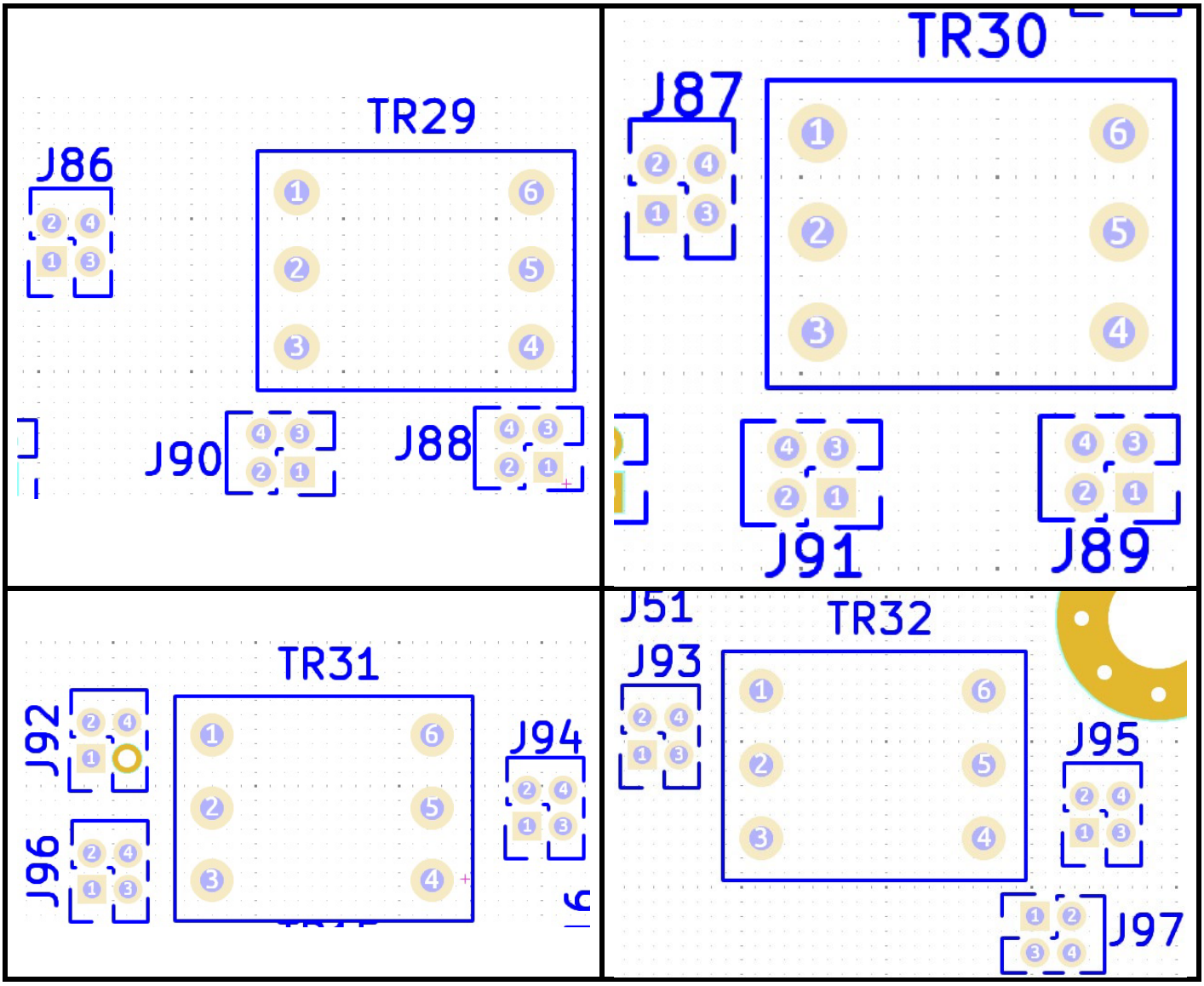


Figure 6





4. Electrical Characteristics

Shows the electrical specifications of the transformers used in this system. All of the transformers have are identical with a 1:1 ratio.

Parameter	**-901**	**-902**
Resistance	10KΩ CT	600Ω CT
Power level	40mW	50mW
Frequency Response	±2.0dB @ 300Hz to 100Khz (1 Khz Ref.)	±3.0dB @ 300Hz to 100Khz (1 Khz Ref.)
Longitudinal Balance	60db Min @ 1Khz	60db Min @ 1Khz
Operating Temp.	-20°C – 80°C	-20°C – 80°C

Table 2

5. Physical Characteristics

5.1 Mounting Dimensions

The Discrete Input Signal Conditioner Board is a 108mm X 128mm card that can be mounted on a DIN rail. Figure 7 shows the mounting dimensions of the board. The device does not have active components, so it doesn't consume quiescent power.

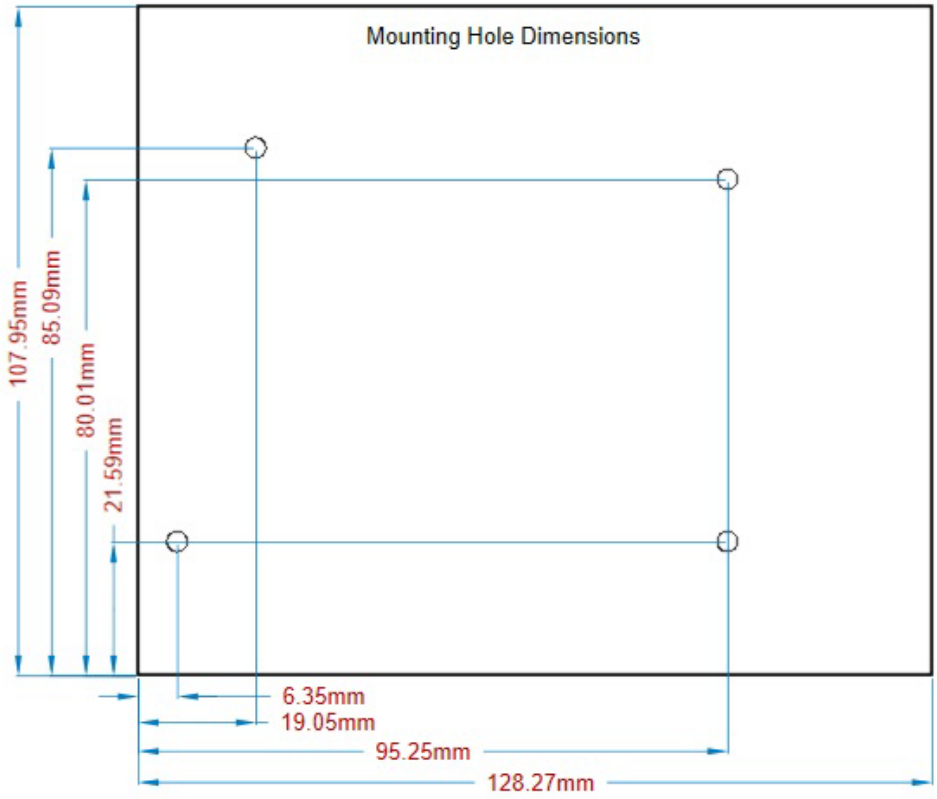


Figure 7

6. J1 Host I/O Connector Pinout

The main host inputs and outputs are connected to connector J1, a 68 Pin AMPLIMITE D-Shaped connector. The connector on the board is TE Connectivity part number 5787170-7. The signals on the user side of the transformers are distributed between three D-Sub connectors. Figure 8 shows the connections on the J1 host connector looking at the connector with the board underneath. Table 3 shows the signals on the pins of J1. The signals on J1 relate directly to the analog interface on a Concurrent Real-Time FPGA board. Cable part number CX-CBL-NPSCA-16-03 and CX-CBL-NPSCA-16-06 allow direct connection between the PCIe FPGA board and the transformer I/Os.

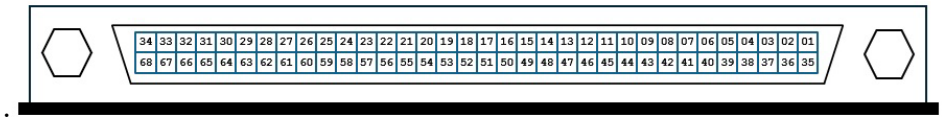


Figure 8

68-Pin J1 Assignment for CQ9500-TR-08					
Pin Number	**Name**	**Description**	**Pin Number**	**Name**	**Description**
01	AI0+	Analog in Ch0+	35	AI0-	Analog in Ch0-
02	AI1+	Analog in Ch1+	36	AI1-	Analog in Ch1-
03	AI2+	Analog in Ch2+	37	AI2-	Analog in Ch2-
04	AI3+	Analog in Ch3+	38	AI3-	Analog in Ch3-
05	AI4+	Analog in Ch4+	39	AI4-	Analog in Ch4-
06	AI5+	Analog in Ch5+	40	AI5-	Analog in Ch5-
07	AI6+	Analog in Ch6+	41	AI6-	Analog in Ch6-
08	AI7+	Analog in Ch7+	42	AI7-	Analog in Ch7-
09	AI8+	Analog in Ch8+	43	AI8-	Analog in Ch8-
10	AI9+	Analog in Ch9+	44	AI9-	Analog in Ch9-
11	AI10+	Analog in Ch10+	45	AI10-	Analog in Ch10-
12	AI11+	Analog in Ch11+	46	AI11-	Analog in Ch11-
13	AI12+	Analog in Ch12+	47	AI12-	Analog in Ch12-
14	AI13+	Analog in Ch13+	48	AI13-	Analog in Ch13-
15	AI14+	Analog in Ch14+	49	AI14-	Analog in Ch14-
16	AI15+	Analog in Ch15+	50	AI15-	Analog in Ch15-

Table 3

68-Pin J1 Assignment for CQ9500-TR-08					
Pin Number	**Name**	**Description**	**Pin Number**	**Name**	**Description**
17	AO0+	Analog out Ch0+	51	AO0-	Analog out Ch0-
18	AO1+	Analog out Ch1+	52	AO1-	Analog out Ch1-
19	AO2+	Analog out Ch2+	53	AO2-	Analog out Ch2-
20	AO3+	Analog out Ch3+	54	AO3-	Analog out Ch3-
21	AO4+	Analog out Ch4+	55	AO4-	Analog out Ch4-
22	AO5+	Analog out Ch5+	56	AO5-	Analog out Ch5-
23	AO6+	Analog out Ch6+	57	AO6-	Analog out Ch6-
24	AO7+	Analog out Ch7+	58	AO7-	Analog out Ch7-
25	AO8+	Analog out Ch8+	59	AO8-	Analog out Ch8-
26	AO9+	Analog out Ch9+	60	AO9-	Analog out Ch9-
27	AO10+	Analog out Ch10+	61	AO10-	Analog out Ch10-
28	AO11+	Analog out Ch11+	62	AO11-	Analog out Ch11-
29	AO12+	Analog out Ch12+	63	AO12-	Analog out Ch12-
30	AO13+	Analog out Ch13+	64	AO13-	Analog out Ch13-
31	AO14+	Analog out Ch14+	65	AO14-	Analog out Ch14-
32	AO15+	Analog out Ch15+	66	AO15-	Analog out Ch15-
33	GNDA	Analog common	67	GNDA	Analog common
34	GNDA	Analog common	68	GNDA	Analog common

Table 3 (cont)

7. P1 I/O Connector Pinout

The P1 male DB37 connector was populated with I/O to optimize resolver simulation. A basic resolver requires one input for stimulus and 2 outputs for return signals. There are 2 sets of this I/O combination on P1. Figure 9 shows the connections on the P1 user connector. Table 4 shows the signals on the pins of P1.

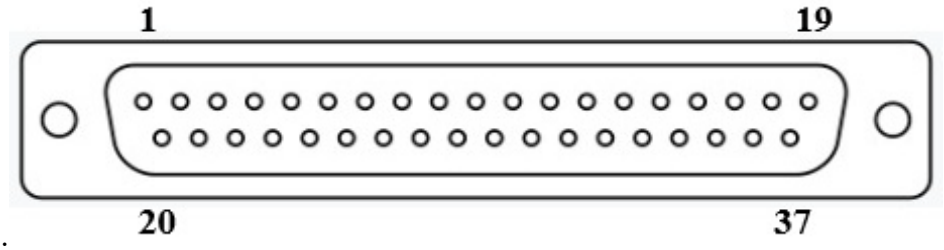


Figure 9

37-Pin P1 Assignment for CQ9500-TR-08					
Pin Number	**Name**	**Description**	**Pin Number**	**Name**	**Description**
1	N/C	N/C	20	N/C	N/C
2	N/C	N/C	21	N/C	N/C
3	N/C	N/C	22	N/C	N/C
4	N/C	N/C	23	N/C	N/C
5	N/C	N/C	24	N/C	N/C
6	UAO12-	Analog out Ch12-	25	UAI6+	Analog in Ch6+
7	UAO12+	Analog out Ch12+	26	UAI6-	Analog in Ch6-
8	UAO13+	Analog out Ch13+	27	UAO13-	Analog in Ch13-
9	N/C	N/C	28	N/C	N/C
10	UAO14-	Analog out Ch14-	29	UAI7+	Analog in Ch7+
11	UAO14+	Analog out Ch14+	30	UAI7-	Analog in Ch7-
12	UAO15+	Analog out Ch15+	31	UAO15-	Analog out Ch15-
13	N/C	N/C	32	N/C	N/C
14	N/C	N/C	33	N/C	N/C
15	N/C	N/C	34	N/C	N/C
16	N/C	N/C	35	N/C	N/C
17	N/C	N/C	36	N/C	N/C
18	N/C	N/C	37	GND	Ground
19	N/C	N/C	Shell	GND	Ground

Table 4

8. P2 I/O Connector Pinout

The P2 male DB37 connector was populated with I/O to optimize resolver simulation. A basic resolver requires one input for stimulus and 2 outputs for return signals. There are 6 sets of this I/O combination on P2. Figure 10 shows the connections on the P2 user connector. Table 5 shows the signals on the pins of P2.

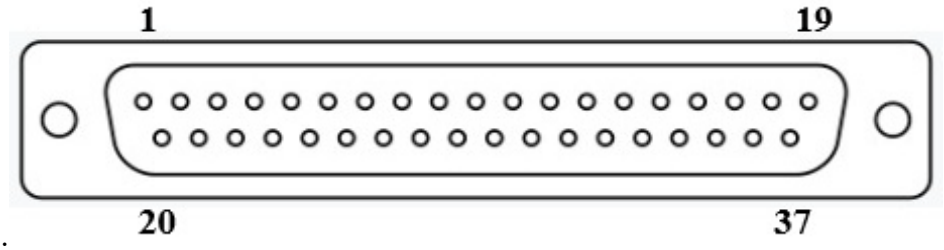


Figure 10

37-Pin P2 Assignment for CQ9500-TR-08					
Pin Number	**Name**	**Description**	**Pin Number**	**Name**	**Description**
19	UAO0+	Analog out Ch0+	37	UAO0-	Analog out Ch0-
18	UAO1-	Analog out Ch1-	36	UAO1+	Analog out Ch1+
17	UAI0-	Analog in Ch0-	35	UAI0+	Analog in Ch0+
16	UAO2+	Analog out Ch2+	34	UAO2-	Analog out Ch2-
15	UAO3-	Analog out Ch3-	33	UAO3+	Analog out Ch3+
14	UAI1-	Analog in Ch1-	32	UAI1+	Analog in Ch1+
13	UAO4+	Analog out Ch4+	31	UAO4-	Analog out Ch4-
12	UAO5-	Analog out Ch5-	30	UAO5+	Analog out Ch5+
11	UAI2-	Analog in Ch2-	29	UAI2+	Analog in Ch2+
10	UAO6+	Analog out Ch6+	28	UAO6-	Analog out Ch6-
9	UAO7-	Analog out Ch7-	27	UAO7+	Analog out Ch7+
8	UAI3-	Analog in Ch3-	26	UAI3+	Analog in Ch3+
7	UAO8+	Analog out Ch8+	25	UAO9+	Analog out Ch9+
6	UAO9-	Analog out Ch9-	24	UAO8-	Analog out Ch8-
5	UAI4+	Analog in Ch4+	23	UAI4-	Analog in Ch4-
4	UAO10+	Analog out Ch10+	22	UAO11+	Analog out Ch11+
3	UAO11-	Analog out Ch11	21	UAO10-	Analog out Ch10-
2	UAI5+	Analog in Ch5+	20	UAI5-	Analog in Ch5-
1	GND	Ground	Shell	GND	Ground

Table 5

9. P3 I/O Connector Pinout

The P3 male DB25 connector was populated with analog inputs. Figure 11 shows the connections on the P3 user connector. Table 6 shows the signals on the pins of P3.

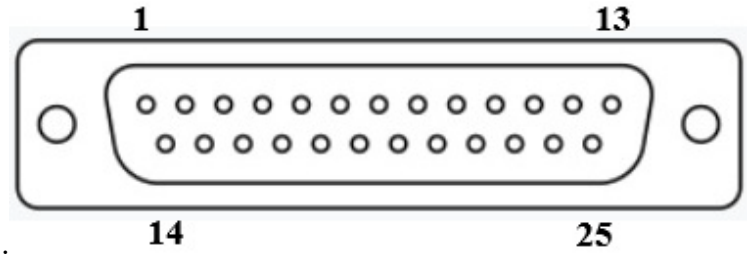


Figure 11

25-Pin P3 Assignment for CQ9500-TR-08					
Pin Number	**Name**	**Description**	**Pin Number**	**Name**	**Description**
1	GND	Ground	14	N/C	N/C
2	UAI8+	Analog in Ch8+	15	UAI8-	Analog in Ch8-
3	UAI9+	Analog in Ch9+	16	UAI9-	Analog in Ch9-
4	UAI10+	Analog in Ch10+	17	UAI10-	Analog in Ch10-
5	UAI11+	Analog in Ch11+	18	UAI11-	Analog in Ch11-
6	UAI12+	Analog in Ch12+	19	UAI12-	Analog in Ch12-
7	UAI13+	Analog in Ch13+	20	UAI13-	Analog in Ch13-
8	UAI14+	Analog in Ch14+	21	UAI14-	Analog in Ch14-
9	UAI15+	Analog in Ch15+	22	UAI15-	Analog in Ch15-
10	N/C	N/C	23	N/C	N/C
11	N/C	N/C	24	N/C	N/C
12	N/C	N/C	25	N/C	N/C
13	N/C	N/C	Shell	GND	Ground

Table 6

10. FPGA Workbench Simulations

The following is a more detailed description of how to interface the CQ9500-TR-08 as part of a CCRT system with angular position measurement sensors such as RVDTs, LVDTs, Resolvers, and Synchros. The transformers are particularly useful simulating these sensors since they are also transformers. The transformers also provide galvanic isolation between the computer simulating the system and between each analog channel.

10.1 System Block Diagram

One transformer CQ9500-TR-08 can support 2 Synchro models or up to 4 sensor simulation models and 4 sensor readers. Figure 12 is a connection diagram of a fully connected system. Depending on the FPGA product, it is possible to use two analog daughter boards to connect to two CQ9500-TR-08 boards thus providing two systems with up to 4 Synchro models or up to 8 sensor simulation models and up to 8 readers supported by one FPGA interface.

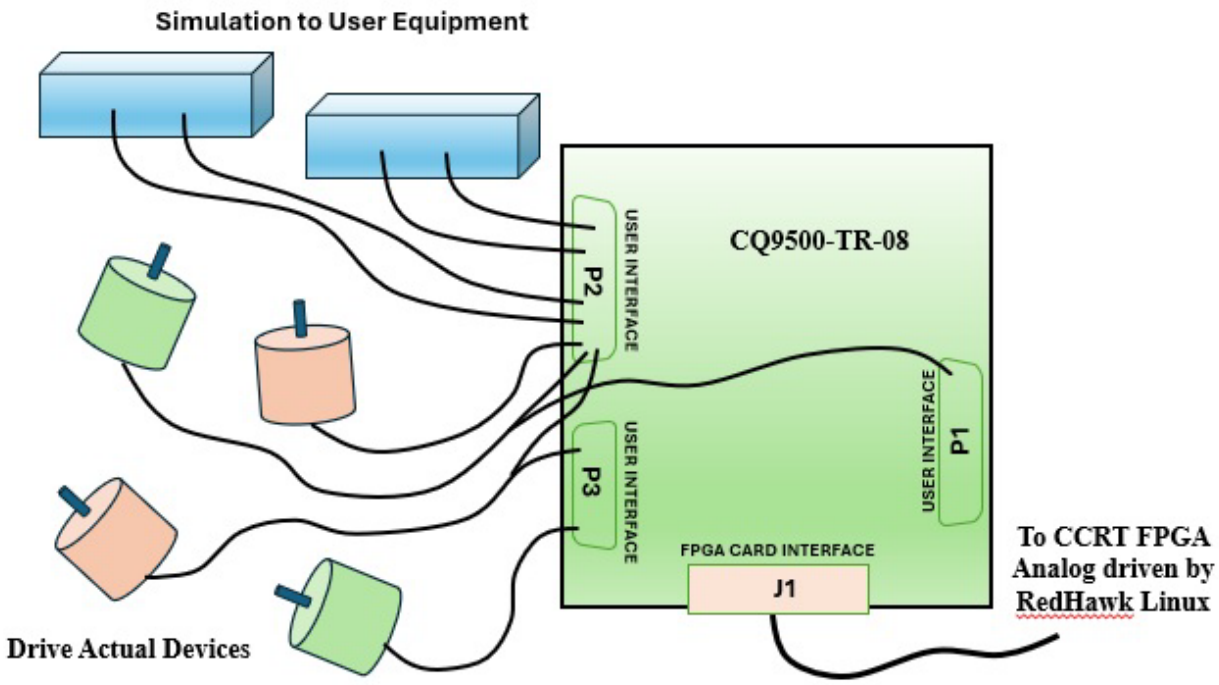


Figure 12

10.2 Standard Support

There are standard I/O assignments for sensor support that line up with device support in FPGA Workbench. Table 7 shows the standard I/O assignments and connections for LVDT, RVDT, and Resolver simulations.

LVDT/ RVDT/ Resolver Simulation I/O						
Description	Signal	Host Positive	Host Negative	Transformer	User Positive	Use Negative
Excitation Ep_1 In	AI CH0	J1-1	J1-35	TR1	P2-35	P2-17
Es21_1 Out	AO CH4	J1-21	J1-55	TR21	P2-13	P2-31
Es22_1 Out	AO CH5	J1-22	J1-56	TR22	P2-30	P2-12
Excitation Ep_2 In	AI CH1	J1-2	J1-36	TR2	P2-32	P2-14
Es21_2 Out	AO CH6	J1-23	J1-57	TR23	P2-10	P2-28
Es22_2 Out	AO CH7	J1-24	J1-58	TR24	P2-27	P2-9
Excitation Ep_3 In	AI CH2	J1-3	J1-37	TR3	P2-29	P2-11
Es21_3 Out	AO CH8	J1-25	J1-59	TR25	P2-7	P2-24
Es22_3 Out	AO CH9	J1-26	J1-60	TR26	P2-25	P2-6
Excitation Ep_4 In	AI CH3	J1-4	J1-38	TR4	P2-26	P2-8
Es21_4 Out	AO CH10	J1-27	J1-61	TR27	P2-4	P2-21
Es22_4 Out	AO CH11	J1-28	J1-62	TR28	P2-22	P2-3

Table 7

Table 8 shows the standard I/O assignments and connections for Synchro simulations.

Synchro Simulation I/O						
Description	Signal	Host Positive	Host Negative	Transformer	User Positive	Use Negative
Excitation Ep_1 In	AI CH0	J1-1	J1-35	TR1	P2-35	P2-17
Es31_1 Out	AO CH3	J1-20	J1-54	TR20	P2-33	P2-15
Es12_1 Out	AO CH4	J1-21	J1-55	TR21	P2-13	P2-31
Es23_1 Out	AO CH5	J1-22	J1-56	TR22	P2-30	P2-12
Excitation Ep_2 In	AI CH1	J1-2	J1-36	TR2	P2-32	P2-14
Es31_2 Out	AO CH6	J1-23	J1-57	TR23	P2-10	P2-28
Es12_2 Out	AO CH7	J1-24	J1-58	TR24	P2-27	P2-9
Es23_2 Out	AO CH8	J1-25	J1-59	TR25	P2-7	P2-24
Excitation Ep_3 In	AI CH2	J1-3	J1-37	TR3	P2-29	P2-11
Es31_3 Out	AO CH9	J1-26	J1-60	TR26	P2-25	P2-6
Es12_3 Out	AO CH10	J1-27	J1-61	TR27	P2-4	P2-21
Es23_3 Out	AO CH11	J1-28	J1-62	TR28	P2-22	P2-3

Table 8

Table 9 shows the standard I/O assignments and connections for LVDT, RVDT, and Resolver readers.

LVDT/ RVDT/ Resolver Reader I/O						
Description	Signal	Host Positive	Host Negative	Transformer	User Positive	Use Negative
Excitation Ep_1 Out	AO CH0	J1-17	J1-51	TR17	P2-19	P2-37
Es21_1 In	AI CH4	J1-5	J1-39	TR5	P2-5	P2-23
Es22_1 In	AI CH5	J1-6	J1-40	TR6	P2-2	P2-20
Excitation Ep_2 Out	AO CH1	J1-18	J1-52	TR18	P2-36	P2-18
Es21_2 In	AI CH6	J1-7	J1-41	TR7	P1-25	P1-26
Es22_2 In	AI CH7	J1-8	J1-42	TR8	P1-29	P1-30
Excitation Ep_3 Out	AO CH2	J1-19	J1-53	TR19	P2-16	P2-34
Es21_3 In	AI CH8	J1-09	J1-43	TR9	P3-2	P3-15
Es22_3 In	AI CH9	J1-10	J1-44	TR10	P3-36	P3-16
Excitation Ep_4 Out	AO CH3	J1-20	J1-54	TR20	P2-33	P2-15
Es21_4 In	AI CH10	J1-11	J1-45	TR11	P3-4	P3-17
Es22_4 In	AI CH11	J1-12	J1-46	TR12	P3-5	P3-18

Table 9

Table 10 shows the standard I/O assignments and connections for Synchro readers.

Synchro Reader I/O						
Description	Signal	Host Positive	Host Negative	Transformer	User Positive	Use Negative
Excitation Ep_1 Out	AO CH0	J1-17	J1-51	TR17	P2-19	P2-37
Es31_1 In	AI CH3	J1-4	J1-38	TR4	P2-26	P2-8
Es12_1 In	AI CH4	J1-5	J1-39	TR5	P2-5	P2-23
Es23_1 In	AI CH5	J1-6	J1-40	TR6	P2-2	P2-20
Excitation Ep_2 Out	AO CH1	J1-18	J1-52	TR18	P2-36	P2-18
Es31_2 In	AI CH6	J1-7	J1-41	TR7	P1-25	P1-26
Es12_2 In	AI CH7	J1-8	J1-42	TR8	P1-29	P1-30
Es23_2 In	AI CH8	J1-09	J1-43	TR9	P3-2	P3-15
Excitation Ep_3 Out	AO CH2	J1-19	J1-53	TR19	P2-16	P2-34
Es31_3 In	AI CH9	J1-10	J1-44	TR10	P3-36	P3-16
Es12_3 In	AI CH10	J1-11	J1-45	TR11	P3-4	P3-17
Es23_3 In	AI CH11	J1-12	J1-46	TR12	P3-5	P3-18

Table 10